UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,434	09/30/2003	Eizi Yokoyama	040894-5652-01	2611

9629 7590 02/19/2009

MORGAN LEWIS & BOCKIUS LLP
1111 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20004

EXAMINER	
PHAN, THIEM D	

ART UNIT	PAPER NUMBER
3729	

MAIL DATE	DELIVERY MODE
02/19/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/673,434	YOKOYAMA ET AL.	
	Examiner	Art Unit	
	THIEM PHAN	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4,7,11 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4,7,11 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/819,694.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on 12/10/08 has been entered.

Specification and Drawings

2. The disclosure is objected to because of the following informalities: on page 10, line 10, the item of circuit board should be 11 instead of 17, since the lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicants' cooperation is requested in correcting any errors of which applicant may become aware in the specification.

As in Figure 3, the two items 15 and 16 should be exchanged for proper reference.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4, 7 and 13 are rejected under 35 U.S.C. 103(a) as being anticipated by Shoji et al (US 5,982,629).

Regarding claim 4, Shoji et et al teach a method of fabricating a circuit board (Col. 3, lines 29+; col. 6, lines 36-40 where the item 1 of Fig. 1 to 6 can be interpreted as of a printed circuit board or component chip), comprising the steps of:

- a step of forming a terminal portion (Fig. 1, 2) in manufacturing a square-shaped circuit board (Fig. 1, 1; col. 7, line 40), said step of forming a terminal portion being to stack a base layer of copper or Cu (Fig. 1, 2; col. 4, lines 45-48) and a plated layer of gold or Au (Fig. 1, 3; col. 2, lines 45 & 46) successively to form the terminal portion; except for having the circuit board made of glass epoxy resin; and
- a step of forming an insulating layer (Fig. 9, 5) after said step of forming a terminal portion in manufacturing said circuit board, said step of forming an insulating layer being to form an insulating layer in the other area than the area where said terminal portion (Fig. 9, 2) is formed,
- wherein said insulating layer is formed so as to cover a peripheral edge of said plated layer (Fig. 9, 3; col. 5, lines 28-30) so that the surface of said circuit board and at least one of the surface of the base layer (Fig. 9, 2) are not exposed externally, and the insulating layer (Fig. 9, 5; col. 11, lines 38 & 39) is made of epoxy resin or the like; and
- a step of mounting an electronic component (Fig. 7, item 11 is construed as component due to similar process forming bump on component or wiring board; col. 6, lines 36-49) after the step of forming the insulating layer, the step of mounting the electronic

component including mounting the electronic component on given position of the circuit board by a solder reflow process (Fig. 7, 8 & 13; col. 9, lines 50-54).

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to have the circuit board made of glass epoxy resin because applicants have not disclose that having the circuit board made of glass epoxy resin provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicants' invention to perform equally well with a silicon substrate material (Abstract) because it insulates and supports the conductive regions (Fig. 1, 2 & 3) as well.

Therefore, it would have been an obvious matter of design choice to modify Shoji et al to obtain the invention as specified in Claim 4.

Regarding claim 7, Shoji et al teach the further steps of:

- forming a base layer of a copper pattern (Fig. 1, 2) on a surface of an insulating board (Fig. 1, 1);
- forming a plated layer (Fig. 1, 3) so as to cover the entire base layer (Fig. 1, 2) by selective plating (Col. 5, line 5); and
- forming an insulating layer (Fig. 9, 5) on said plated layer (Fig. 9, 3) and patterning said insulating layer so that only a portion of said plated layer is exposed externally.

Regarding claim 13, Shoji et et al teach a method of fabricating a circuit board (Col. 3, lines 29+; col. 6, lines 36-40 where the item 1 of Fig. 1 to 6 can be interpreted as of a printed circuit board or component chip), comprising the steps of:

- a step of forming a terminal portion (Fig. 1, 2) in manufacturing a square-shaped circuit board (Fig. 1, 1; col. 7, line 40), said step of forming a terminal portion being to stack a base layer of copper or Cu (Fig. 1, 2; col. 4, line 58), a first plated layer of nickel (Fig. 2, 4) and a second plated layer of gold or Au (Fig. 1, 3; col. 4, line 63) successively to form the terminal portion; except for having the circuit board made of glass epoxy resin; and
- a step of forming an insulating layer (Fig. 9, 5) after said step of forming a terminal portion in manufacturing said circuit board, said step of forming an insulating layer being to form an insulating layer in the other area than the area where said terminal portion (Fig. 9, 2) is formed,
- wherein said insulating layer is formed so as to cover a peripheral edge of said plated layer (Fig. 9, 3; col. 5, lines 28-30) so that the surface of said circuit board and at least one of the surface of the base layer (Fig. 9, 2) are not exposed externally, and the insulating layer (Fig. 9, 5; col. 11, lines 38 & 39) is made of epoxy resin or the like; and
    - further forming the base layer pattern (Fig. 2, 2) on a surface of the insulating board (1);
    - further forming the first plated layer (4) so as to cover the entire base layer by selective plating; and
    - further forming the second plated layer (3) so as to cover the entire first plated layer by selective plating; and
    - further forming the insulating layer (Fig. 9, 5) on the second plated layer and patterning the insulating layer so that only a portion of the second plated layer is exposed externally; and

- a step of mounting an electronic component (Fig. 7, item 11 is construed as component due to similar process forming bump on component or wiring board; col. 6, lines 36-49) after the step of forming the insulating layer, the step of mounting the electronic component including mounting the electronic component on given position of the circuit board by a solder reflow process (Fig. 7, 8 & 13; col. 9, lines 50-54).

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to have the circuit board made of glass epoxy resin because applicants have not disclose that having the circuit board made of glass epoxy resin provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicants' invention to perform equally well with a silicon substrate material (Abstract) because it insulates and supports the conductive regions (Fig. 1, 2 & 3) as well.

Therefore, it would have been an obvious matter of design choice to modify Shoji et al to obtain the invention as specified in Claim 13.

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being anticipated by Shoji et al in view of Mita et al (US 6,297,142).

Shoji et al teach a method of fabricating a circuit board, which reads on applicants' claimed invention; except for stamping out a rigid-type integral along each area, on which the circuit board is to be formed, with a mold.

Mita et al teach a method of forming semiconductor chip (Figs. 10A-11D; 1) by stamping out a rigid-type integral along each area of the TAB (Fig. 11A, 6) on which the circuit board is to

be formed, with a mold (Fig. 11D, S805; col. 6, lines 43-45), in order to mass produce the chip components.

It would be obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Shoji et al by applying the stamping process, as taught by Mita et al, in order to mass produce the chip components.

Response to Arguments

6. Applicants' arguments filed on 12/10/08 have been fully considered but they are not persuasive.

Applicants' assertions that the prior art Shoji et al fails to teach a step of mounting an electronic component on the circuit board by a solder reflow process (Remarks, page 7) are traversed because Shoji et al do teach the step of mounting an electronic component (Fig. 7, item 11 is construed as component due to similar process forming bump on component or wiring board; col. 6, lines 36-49) after the step of forming the insulating layer, the step of mounting the electronic component including mounting the electronic component on given position of the circuit board by a solder reflow process (Fig. 7, 8 & 13; col. 9, lines 50-55). Again, in a further response to these remarks, the examiner needs to emphasize that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims, which are judged with their broadest reasonable interpretation. (See MPEP 2111 and In re Geuns, 26 USPQ 2nd 1057 (Fed. Cir. 1993)). Therefore, the prior art Shoji et al at a minimum teach the claimed limitation of the solder reflow of a component to the pattern wiring after the insulation layer is formed.

Furthermore, applicants cite the replacement sheet drawing of Figure 3 (Remarks, page 6) but it is not filed in this amendment.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim Phan whose telephone number is 571-272-4568. The examiner can normally be reached on M & Tu, 6AM - 2PM, and W & Th, 9AM – 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Bryant can be reached on 571-272-4526. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Phan Thiem/
Primary Examiner, Art Unit 3729

February 16, 2009